UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/609,216 | 06/26/2003 | Karl H. Mauritz | 42P16326 | 6486 |

8791 7590 11/16/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

| EXAMINER | |
|---|---|
| PATEL, HETUL B | |
| ART UNIT | PAPER NUMBER |
| 2186 | |

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED

NOV 1 6 2006

Technology Center 2100

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/609,216
Filing Date: June 26, 2003
Appellant(s): MAURITZ ET AL.

Gordon R. Lindeen III
<u>For Appellant</u>

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed on October 16, 2006 appealing from the Office action mailed March 14, 2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 6,862,185 | Morris | 03-2005 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

A. Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added limitation in independent claims 1, 14 and 27, "the resistive bus splitter having a specific resistance for each memory module" is not properly described or supported by the application as filed. Although paragraphs [0024] and [0025] of the specification discloses having a specific impedance for each memory module, that is not necessarily same having resistance for each memory module as claimed because impedance is not only depends on resistance but also on frequency. So unless the frequency is constant, resistance is not same as impedance. Claims 2-13, 15-26 and 28-30 are also rejected based on the same rationale as they depend upon the rejected base claims.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

B. Claims 1, 4, 7-8, 14, 17 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Morris (USPN: 6,862,185).

As per claim 1, Morris teaches a circuit (i.e. 200 in Fig. 2) comprising: a plurality of memory modules (i.e. 201 in Fig. 2); a memory controller (i.e. 207 in Fig. 2) coupled to the plurality of memory modules; a resistive bus splitter coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller (i.e. embedded in the memory board 203 to split the signals sent from high speed connectors 205 and 209 into plurality of connectors 202 coupled to the memory modules 201 in Fig. 2); and a plurality of terminators (i.e. 204, 210 in Fig. 2) to reduce signal reflections corresponding to the split signals (e.g. see Col. 4, 14-17 and Fig. 2). Furthermore, the resistive bus splitter in the circuit taught by Morris has to have a specific resistance for each memory module because even if each memory module is connected thru a piece of wire, it still has a resistance as claimed.

As per claim 4, Morris teaches the claimed invention as described above and furthermore, Morris teaches that the memory modules (i.e. 201 in Fig. 2) are dual in-line memory modules (DIMMs) (e.g. see Col. 3, lines 46-47 and Fig. 2).

As per claim 7, Morris teaches the claimed invention as described above. The further limitation of selecting miniature integrated resistor packs as the resistive bus splitter is inherently taught by Morris. The miniature integrated resistor packs has to be present in the memory board (i.e. 203 in Fig. 3A) in order to reduce the noise in the signals sent to DIMMs.

As per claim 8, Morris teaches the claimed invention as described above and furthermore, Morris teaches a plurality of memory expander chips (MXCs) (i.e. 201-1 and 201-2 in Fig. 3) coupled between the resistive bus splitter (i.e. embedded in 203 in Fig. 2) and the plurality of memory modules (i.e. 201 in Fig. 2) (e.g. see Fig. 2).

As per claims 14, 17 and 20-21, see arguments with respect to the rejection of claims 1, 4 and 7-8, respectively. Claims 14, 17 and 20-21 are also rejected based on the same rationale as the rejection of claims 1, 4 and 7-8, respectively.

As per claim 19, Morris teaches the claimed invention as described above and furthermore, Morris teaches that the resistive bus splitter includes a miniature resistive splitter on a PCB (i.e. a plurality of resistors in order to reduce the noise in the signals sent to DIMMs are *inherently embedded* on the memory board 203 in Fig. 2) (e.g. see Fig. 2).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

C. Claims 2-3 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris.

As per claims 2 and 3, Morris teaches the claimed invention as described above and furthermore, Morris teaches that the plurality of terminators (i.e. 204, 210 in Fig. 2) are attached/mounted on the memory board 203 in Fig. 2. Official notice is taken of the prior art teaching a plurality of components (i.e. terminators) on a single chip. First of all, it has been held that to make integral is not generally given patentable weight. Note In re Larson 144 USPQ 347 (CCPA 1965). Furthermore In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) states that to integrate electrical components onto a unitary, one piece structure would be obvious. Integrating/embedding multiple components on a single chip reduces cabling problems, reduces latency required for communicating among processors, improves efficiency of message passing, reduces chip-to-chip communications costs, allows for less pin count, area saving and high speed data transfer between the elements and leads to further power efficiency and increased scalability. Because multiple terminators embedded on the memory module/memory controller provides improvements in efficiency, cost and scalability over terminators mounted on a circuit board(s), it would have been obvious to use a single chip design in

the device of Morris. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

As per claims 15-16, see arguments with respect to the rejection of claims 2 and 3, respectively. Claims 15-16 are also rejected based on the same rationale as the rejection of claims 2 and 3, respectively.

D. Claims 8-13 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Talbot et al. (USPN: 2005/0166006) hereinafter, Talbot.

As per claim 8, Morris teaches the claimed invention as described above and furthermore, Morris teaches a plurality of memory expander chips (MXCs) (i.e. 201-1 and 201-2 in Fig. 3) coupled between the memory controller (i.e. 207 in Figs. 2-3) and the plurality of memory modules. Suppose even if Morris does not specifically define 201-1 and 201-2 in Fig. 3 as a plurality of memory expander *chips* (MXCs) as claimed, Talbot, on the other hand, teaches a plurality of memory expander chips (MXCs) (i.e. the memory control hubs 160A-160B in Fig. 1) coupled between the memory controller (i.e. 106 in Fig. 1) and the plurality of memory modules (i.e. 171A-171N in Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to include a plurality of memory expander chips taught by Talbot in the circuit taught by Morris. In doing so, a large number of memory modules can be connected to the circuit. Therefore, it is being advantageous. Furthermore, in doing so, address signals are sent through a plurality of MXCs between the resistive bus splitter and the plurality of memory modules.

As per claim 9, the combination of Morris and Talbot teaches the claimed invention as described above and furthermore, Talbot teaches that the plurality of MXCs (i.e. 160A-160B in Fig. 1) enable access to relative larger memory arrays (i.e. 171A-171N and 181A-181N in Fig. 1).

As per claim 10, the combination of Morris and Talbot teaches the claimed invention as described above and furthermore, Talbot teaches that each of the plurality of MXCs (i.e. 160A-160B in Fig. 1) include a built in bi-directional cache (i.e. the cache 175A, 175B in Fig. 1) to decrease latency and increase throughput efficiency (e.g. see Fig. 1).

As per claim 11, the combination of Morris and Talbot teaches the claimed invention as described above. The further limitation, of having a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported DIMMs, is also *inherently* taught by Talbot because by coupling a MXC (i.e. 201-1 in Fig. 3) between a plurality (i.e. two) of memory modules/DIMMs (i.e. 201 in Fig. 2), the bandwidth gets doubled compared to if a DIMM is directly connected to the controller (i.e. 207 in Figs. 2-3) (e.g. see Figs. 2-3).

As per claim 12, the combination of Morris and Talbot teaches the claimed invention as described above and furthermore, Talbot teaches about having access coalescing functionality (i.e. access uniting) in each of the plurality of MXCs (i.e. 160A and 160B in Fig. 1). For example, accesses from a plurality of memory chips (i.e. 171A-171N in Fig. 1) are coalesced/gathered by the hub 160 A (e.g. see Fig. 1).

As per claim 13, the combination of Morris and Talbot teaches the claimed invention as described above and furthermore, Talbot teaches that a portion of the plurality of MXCs (i.e. 160A-160B in Fig. 1) are coupled to each other in series (e.g. see Fig. 1).

As per claims 21-26, see arguments with respect to the rejection of claims 8-13, respectively. Claims 21-26 are also rejected based on the same rationale as the rejection of claims 8-13, respectively.

E. Claims 5-6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Jeddeloh et al. (USPN: 2004/0044933) hereinafter, Jeddeloh.

As per claim 5, Morris teaches the claimed invention as described above, but Morris failed to teach that the circuit further including a reference voltage generator to generate a reference voltage corresponding to a memory chip voltage. Jeddeloh discloses a reference voltage generator (i.e. the combination of 74 and 76 in Fig. 2), which generates a reference voltage (i.e. $V_{Ref}$) corresponding to a memory chip voltage (e.g. see paragraph [0025] and Fig. 2). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the reference voltage generator taught by Jeddeloh in Morris's circuit. In doing so, the memory modules 60a, 60b may use the reference voltage Vref to determine data bit values during data sensing, writing and reading operations.

As per claim 6, the combination of Morris and Jeddeloh teaches the claimed invention as described above and furthermore, Jeddeloh teaches that the reference

voltage (i.e. $V_{Ref}$) is provided to the plurality of memory modules (i.e. 60a and 60b in Fig. 2) and the memory controller (i.e. 100 in Fig. 2) (e.g. see paragraph [0025] and Fig. 2).

As per claims 18, see arguments with respect to the rejection of claims 5 and 6. Claim 18 is also rejected based on the same rationale as the rejection of claims 5 and 6.

F. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freker (USPN: 6,442,645) in view of Morris.

As per claim 27, Freker teaches a computer system (i.e. 100 in Fig. 1) comprising: a central processing unit (CPU) (i.e. the processor 105 in Fig. 1); a display device (i.e. 125 in Fig. 1) coupled to the CPU to display an image; a plurality of memory modules (i.e. the memory array 120 in Figs. 1-2); a memory controller (i.e. 116 in Fig. 2) coupled to the plurality of memory modules (i.e. $210_{1-4}$ in Fig. 2) and the CPU (e.g. see Figs. 1-2). However, Freker does not clearly disclose a plurality of bus splitters and a plurality of terminators. Morris, on the other hand, teaches a plurality of bus splitters coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller (i.e. embedded in the memory board 203 to split the signals sent from high speed connectors 205 and 209 into plurality of connectors 202 coupled to the memory modules 201 in Fig. 2); and a plurality of terminators (i.e. 204, 210 in Fig. 2) to reduce signal reflections corresponding to the split signals (e.g. see Col. 4, 14-17 and Fig. 2). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement a plurality of bus splitters and a plurality of

terminators of Morris in the computer system taught by Freker. By implementing bus splitters, the signals from the memory controller can be split and then sent to a plurality of memory modules at the same time and by implementing terminators, signal reflections can be reduced or totally avoided. Therefore, it is being advantageous.

As per claim 28, the combination of Freker and Morris teaches the claimed invention as described above. The further limitation of selecting miniature integrated resistor packs as the resistive bus splitter is inherently taught by Morris. The miniature integrated resistor packs has to be present in the memory board (i.e. 203 in Fig. 3A) in order to reduce the noise in the signals sent to DIMMs.

As per claim 29, the combination of Freker and Morris teaches the claimed invention as described above and furthermore, Morris teaches that the system further including a plurality of memory expander chips (i.e. 201-1 and 201-2 in Fig. 3) coupled between the resistive bus splitter (i.e. embedded in the memory board 203 to split the signals sent from high speed connectors 205 and 209 into plurality of connectors 202 coupled to the memory modules 201 in Fig. 2) and the plurality of memory modules (i.e. 201 in Fig. 2) to perform memory functions independent of the memory controller (i.e. 207 in Fig. 2) (e.g. see Figs. 2-3).

G. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freker (USPN: 6,442,645) in view of Morris, further in view of Nizar et al. (USPN: 6,889,284) hereinafter, Nizar.

As per claim 30, the combination of Freker and Morris teaches the claimed invention as described above. However, none of them teaches that the MXC functions include at least one of refresh, dynamic address space re-mapping and memory POST. Nizar, however, teaches that the MXC (i.e. the memory translator hub 100 in Fig. 1) functions include refresh operation (e.g. see claim 9 and Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the computer system taught by the combination of Freker and Morris as taught by Nizar so the MXC can perform the refresh operation on memory modules. In doing so, the main controller (i.e. the processor 130 in Fig. 1) can be relieved from the burden of refreshing all the memory modules connected to it. Therefore, the overall performance of the computer system improves.

**(10) Response to Argument**

**Appellant's arguments:**

A. The resistors Rs clearly show a resistance sufficient to support a claim to "having a specific resistance" as claimed in claim 1.
B. Absent any teaching of how signals are distributed "a resistive bus splitter having a specific resistance (or impedance) for each memory module" as recited in claim 1 is not anticipated.

**Examiner's response:**

In response to Appellant's argument **A**, Examiner would like to clarify that the resistors Rs shown in Fig. 2 are not sufficient to support the limitation "having a specific resistance" of claim 1 because in the description of the Fig. 2, in the specification, the Rs is defined as

- Rs = ((n-1)*Zo)/(n+1), where n = the number of splitter segments (where n = 4 for the embodiment of the present invention shown in Fig. 2 (i.e., one driver input with four (n) receiver outputs));

wherein the Zo is defined as

Zo = transmission line impedance (e.g., 55 Ω +/- 10%).

Therefore, Rs in Fig. 2 is not "pure" resistance but it is impedance. Furthermore, paragraphs [0024] and [0025] of the specification clearly discloses having a specific impedance for each memory module. This is not necessarily same having resistance for each memory module as claimed because impedance is not only depends on resistance but also on frequency. So unless the frequency is constant, resistance is not same as impedance.

In response to Appellant's argument **B**, Examiner would like to point out to Appellant that even though the Morris reference does not specifically show a resistive bus splitter, it has to be inherently present in the circuit shown in Fig. 2 of Morris because if the data/address/signal are sent thru a common bus to a plurality of memory modules, the circuit would not function correctly due to data corruption. Therefore, in

the Morris prior art, signals have to be split and separately sent out to different memory modules 201 shown in Fig. 2.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

H.B. Patel
Hetul Patel
Examiner
Art Unit 2186

Conferees:

Lynne Browne
TC2100

**Lynne H. Browne**
**Appeal Specialist, TQAS**
**Technology Center 2100**

Matt Kim
SPE, AU 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100